AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Previously Presented) A bus framer comprising:

an engine which extracts information from a frame of data being transmitted over a time-division multiplexed bus, wherein the frame of data comprises a data structure having blocks arranged in N rows and M columns, where N and M are integers that are greater than one, a block including data used to implement a bus frame protocol and designating a destination port of a receiving device and a time slot for the data; and

a processor which receives the information from the engine over an internal bus and forwards the information.

2. (Original) The bus framer of claim 1, further comprising:

a mapper which maps the frame of data on the time-division multiplexed bus to a read/write bus; and

a functional module which receives data from the read/write bus and which handles the data.

3. (Original) The bus framer of claim 2, wherein the time-division multiplexed bus, the internal bus, and the read/write bus all run off the same clock.

4. (Original) The bus framer of claim 1, further comprising:

a storage medium for storing the information in a database; and

an interface module which provides a link to an external device;

wherein the processor forwards the information to at least one of the storage medium and the interface module.

5. (Original) The bus framer of claim 1, further comprising:

a framing engine which generates the frame and outputs the frame to the time-division multiplexed bus.

6. (Previously Presented) The bus framer of claim 5, wherein the framing engine stores the frame in memory prior to outputting the frame.

7. (Original) The bus framer of claim 1, wherein the engine comprises one of (a) a signaling engine which extracts signaling information from the frame, (b) an alarms engine which extracts alarm codes from the frame, (c) a facility data link engine which extracts messages from the frame, and (d) an overhead engine which extracts overhead bits from the frame.

8. (Original) The bus framer of claim 2, wherein the functional module comprises one of (a) a scalar high-speed bus, (b) a slip buffer which stores data temporarily to accommodate frequency and phase differences between a clock of the bus framer and external clock domains, (c) a system backplane with a connection to an external device, (d) a bit error rate testing generator/analyzer, and (e) a high-speed data link controller.

9. (Currently Amended) The bus framer of claim 1, further comprising:

a read/write bus;

~~plural~~ a plurality of functional modules which communicate with the engine via the read/write bus; and

an arbiter which regulates access of the ~~plural~~ plurality of functional modules to the read/write bus.

10. (Currently Amended) The bus framer of claim 9, wherein the arbiter grants a first of the ~~plural~~ plurality of functional modules access to the read/write bus in a first bus cycle, and grants a second of the ~~plural~~ plurality of functional modules access to the read/write bus in a second bus cycle, the second bus cycle immediately following the first bus cycle.

11. (Previously Presented) A method comprising:

using an engine to extract information from a frame of data being transmitted over a time-division multiplexed bus, wherein the frame of data comprises a data structure having

blocks arranged in N rows and M columns, where N and M are integers that are greater than one, a block including data used to implement a bus frame protocol and designating a destination port of a receiving device and a time slot for the data; and

receiving the information from the engine over an internal bus and forwarding the information.

12. (Original) The method of claim 11, further comprising:

mapping the frame of data on the time-division multiplexed bus to a read/write bus; and

forwarding the frame of data, over the read/write bus, to a functional module which handles the data.

13. (Original) The method of claim 12, wherein the time-division multiplexed bus, the internal bus, and the read/write bus all run off the same clock.

14. (Original) The method of claim 11, further comprising:

storing the information in a database on a storage medium;

wherein the information is forwarded to at least one of the storage medium and an external device.

15. (Original) The method of claim 11, further comprising:

generating the frame; and

outputting the frame to the time-division multiplexed bus.

16. (Previously Presented) The method of claim 15, further comprising storing the frame in memory prior to outputting the frame.

17. (Original) The method of claim 11, wherein the engine comprises one of (a) a signaling engine which extracts signaling information from the frame, (b) an alarms engine which extracts alarm codes from the frame, (c) a facility data link engine which extracts messages from the frame, and (d) an overhead engine which extracts overhead bits from the frame.

18. (Original) The method of claim 12, wherein the functional module comprises one of (a) a scalar high-speed bus, (b) a slip buffer which stores data temporarily to accommodate frequency and phase differences between an internal clock and external clock domains, (c) a system backplane with a connection to an external device, (d) a bit error rate testing generator/analyzer, and (e) a high-speed data link controller.

19. (Currently Amended) The method of claim 11, further comprising:

regulating access of ~~plural~~ a plurality of functional modules to a read/write bus over which communications are exchanged with the engine.

20. (Currently Amended) The method of claim 19, wherein regulating comprises:

granting a first of the ~~plural~~ plurality of functional modules access to the read/write bus in a first bus cycle; and

granting a second of the ~~plural~~ plurality of functional modules access to the read/write bus in a second bus cycle, the second bus cycle immediately following the first bus cycle.

21. (Previously Presented) An article comprising a machine-readable medium that stores executable instructions, the instructions causing a machine to:

extract information from a frame of data being transmitted over a time-division multiplexed bus, wherein the frame of data comprises a data structure having blocks arranged in N rows and M columns, where N and M are integers that are greater than one, a block including data used to implement a bus frame protocol and designating a destination port of a receiving device and a time slot for the data; and

receive the information over an internal bus and forward the information.

22. (Original) The article of claim 21, further comprising instructions to:

map the frame of data on the time-division multiplexed bus to a read/write bus; and

forward the frame of data, over the read/write bus, to a functional module which handles the data.

23. (Original) The article of claim 22, wherein the time-division multiplexed bus, the internal bus, and the read/write bus all run off the same clock.

24. (Original) The article of claim 21, further comprising instructions to:

store the information in a database on a storage medium;

wherein the information is forwarded to at least one of the storage medium and an external device.

25. (Original) The article of claim 21, further comprising instructions to:

generate the frame; and

output the frame to the time-division multiplexed bus.

26. (Previously Presented) The article of claim 25, further comprising instructions to store the frame in memory prior to outputting the frame.

27. (Original) The article of claim 21, wherein the information is extracted using an engine, the engine comprising one of (a) a signaling engine which extracts signaling information from the frame, (b) an alarms engine which extracts alarm codes from the frame, (c) a facility data link engine which extracts messages from the frame, and (d) an overhead engine which extracts overhead bits from the frame.

28. (Original) The article of claim 22, wherein the functional module comprises one of (a) a scalar high-speed bus, (b) a slip buffer which stores data temporarily to accommodate frequency and phase differences between an internal clock and external clock domains, (c) a system backplane with a connection to an external device, (d) a bit error rate testing generator/analyzer, and (e) a high-speed data link controller.

29. (Currently Amended) The article of claim 21, further comprising instructions to:

regulate access of ~~plural~~ a plurality of functional modules to a read/write bus over which communications are exchanged with the engine.

30. (Currently Amended) The article of claim 29, wherein regulating comprises:

granting a first of the ~~plural~~ plurality of functional modules access to the read/write bus in a first bus cycle; and

granting a second of the ~~plural~~ plurality of functional modules access to the read/write bus in a second bus cycle, the second bus cycle immediately following the first bus cycle.